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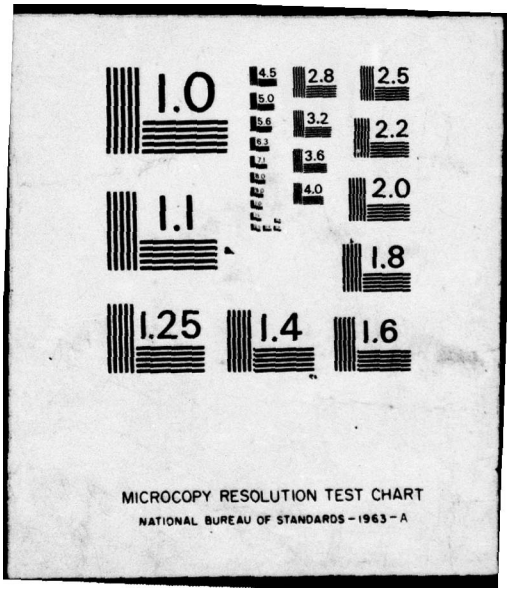
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ANNUAL REPORT NO. 1

Noncoplanar High Power FET

December 19, 1975

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This research was sponsored by
the Office of Naval Research
under contract N00014-75-C-0303,
Contract Authority: NR 251-018/10-23-75

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REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER	2. GOVT ACCESSION NO. (9)
3. RECIPIENT'S CATALOG NUMBER: Rept. no. 1 (Annual)	
4. TITLE (and Subtitle): NONCOPLANAR HIGH POWER FET, (6)	5. TYPE OF REPORT & PERIOD COVERED: Annual Report No. 1 Dec. 74-Dec. 75
	6. PERFORMING ORG. REPORT NUMBER (2)
7. AUTHOR(s): D. R. Decker S. G. Bandy (10)	8. CONTRACT OR GRANT NUMBER(s): N00014-75-C-0303 new (15)
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Varian Associates, 611 Hansen Way, Palo Alto, CA 94303	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: PE 6276N (12) RF-54-581-001, NR 251-018
11. CONTROLLING OFFICE NAME AND ADDRESS: Office of Naval Research, 800 N. Quincy Street, Arlington, VA 22217	12. REPORT DATE: December 19, 1975
	13. NUMBER OF PAGES: 28
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) (11) 19 Dec 75 (12) 30p.	15. SECURITY CLASS. (of this report): UNCLAS
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for Public Release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report) (16) F54581 (17) RF54581001

18. SUPPLEMENTARY NOTES

ONR Scientific Officer
Tel (202) 692-4218

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Noncoplanar FET
Power FET
AlGaAs substrate
GaAs regrowth
Insulating GaAs growth

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Buried-insulating-layer, noncoplanar FETs have been fabricated by growth of insulating regions into n^+ GaAs substrates and subsequent processing to produce transistors for which the substrate becomes the common source electrode. These devices were operated as amplifiers up to 7 GHz, trap-filled-limit (TFL) breakdown was observed for the O_2-doped insulating material with the drain biased positive.

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SUMMARY

Two fundamental approaches to fabrication of noncoplanar FETs have been considered. Primary effort was directed toward development of the buried-insulating-layer, noncoplanar FET. The aspects of buried-insulating layer technology, hole etching, regrowth, and polishing, have been highly developed. Noncoplanar FETs have been fabricated with the buried-insulating-layer technology. These transistors have been characterized by curve tracing, microwave network analysis, amplifier measurements, and other techniques. The best amplifier performance obtained for these devices was 5.2 dB gain at 7 GHz. The characteristics and performance of the noncoplanar FETs tested is analyzed with regard to materials properties obtainable for the buried insulating layer and interface.

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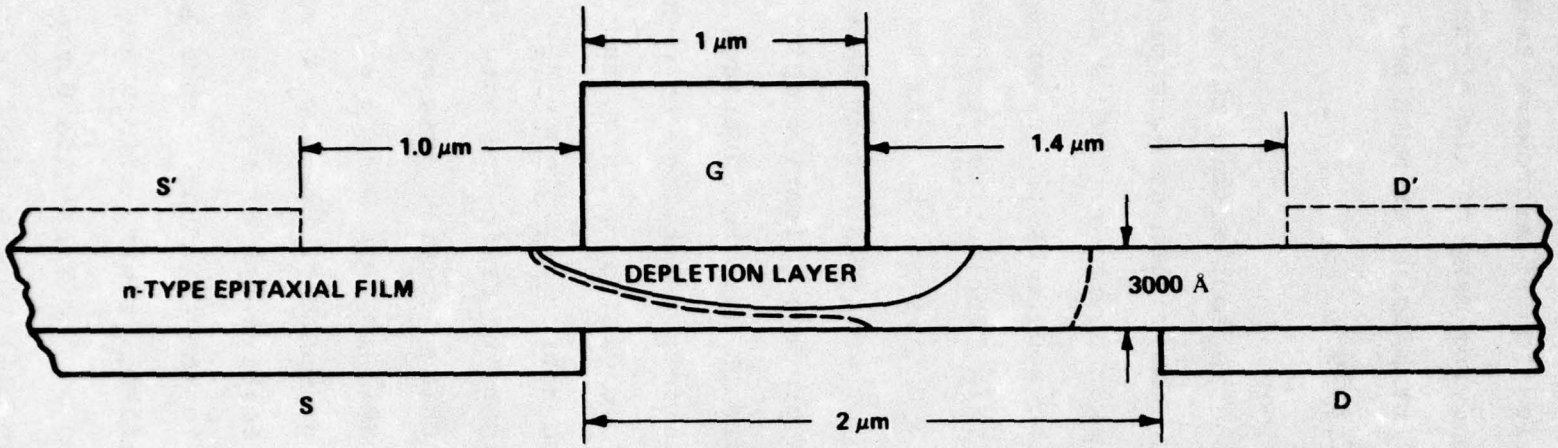
1. INTRODUCTION

One major limitation of present low-noise FET designs is the fact that the source, drain, and gate electrodes are all coplanar and lie on the top surface of the wafer. Freeing the FET design from the constraint of coplanar electrodes leads to many potential improvements through reduction of parasitic elements and ease of device paralleling to obtain high power output. The objective of this program has been to develop designs, techniques, and technology for fabrication of non-coplanar GaAs field effect transistors for operation at X-band and higher frequencies with reduced noise and increased power output.

Two basic approaches to fabrication of noncoplanar FETs which were given serious consideration will be summarized. Materials and device technology developed to make the buried-insulating-layer, noncoplanar FET will be discussed. The results of characterization and evaluation of buried-insulating-layer, noncoplanar FETs will be examined, and some suggestions for the course of future work in this area will be presented.

2. TECHNIQUES FOR FABRICATION OF NONCOPLANAR FETs

Many elements of fabrication technology of noncoplanar FETs such as ohmic contacts, metal lifting, Schottky barrier formation, etc. are common to the technology of low-noise, coplanar FETs. However, two fundamentally different approaches to obtaining noncoplanar geometry have been considered in this laboratory. the first approach is based upon the existence of highly differential etches that distinguish between GaAs and $Al_xGa_{1-x}As$ ($x \geq 0.25$) and the low temperature glass-sealing technology developed for photocathodes at Varian. Briefly, the first approach involves formation of ohmic source and drain contacts on the epitaxial top surface, sealing of this surface to a dielectric support substrate using low temperature glass, removal of the GaAs substrate using differential etching, and finally formation of the Schottky barrier gate on the surface of the epitaxial layer opposite to (and aligned with) the source and drain electrodes. This approach has the significant advantages of being fully noncoplanar as shown in Fig. 1. The primary advantages are the possibility of use of a low-dielectric constant substrate and positioning of the gate opposite both source and drain for reduced parasitics, shorter channel length, and increased breakdown voltages. A disadvantage is the necessity for simultaneously developing and applying the new technologies of glass sealing, growth of FET quality GaAs layers on AlGaAs,



EXPANDED VIEW: (a) S' AND D', COPLANAR SOURCE AND DRAIN LOCATIONS, SPACING ABOUT 3.4 μm

(b) S AND D, NONCOPLANAR SOURCE AND DRAIN LOCATIONS, SPACING ABOUT 2.0 μm

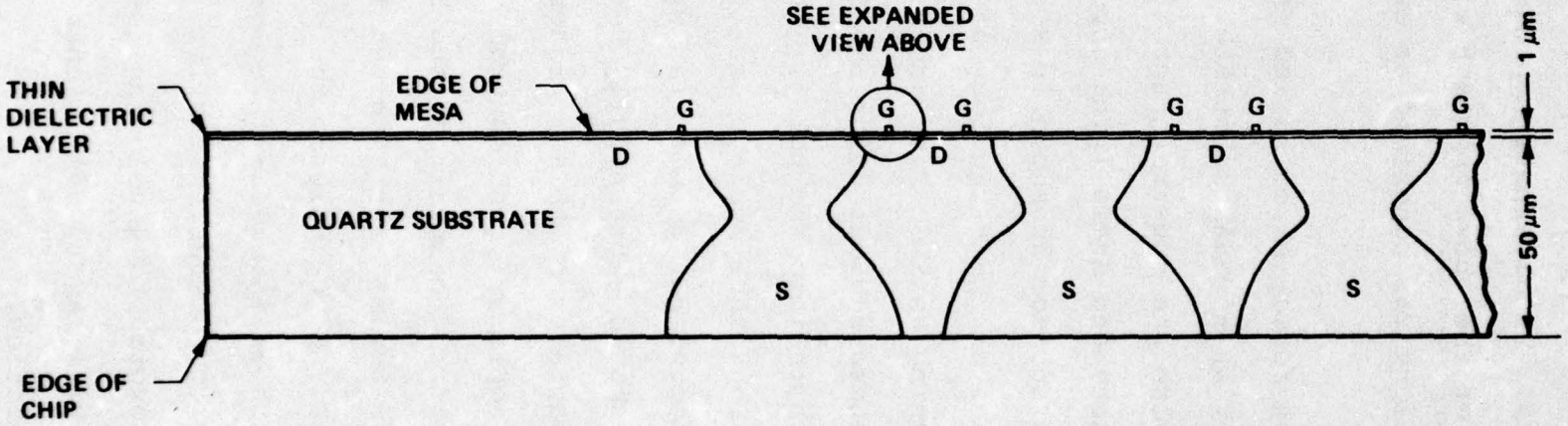


Fig. 1. Cross-sectional view of fully noncoplanar geometry (approximately to scale). [N-type epitaxial layer is too thin to see in lower view.]

and differential etching to the fabrication of microwave transistors. An alternate approach, embodying many of the advantages of the above approach without introducing as much new technology was conceived as outlined below.

The formation of buried insulating regions within the surface of an n^+ GaAs substrate permits fabrication of noncoplanar FETs with the substrate acting as common source electrode and with gate and drain lying opposite the source on the upper epitaxial surface as shown in Fig. 2. This fabrication approach is based on the technology of etching basins in the GaAs surface using an SiO_2 mask and regrowth of semi-insulating GaAs into these regions using the SiO_2 to provide selective epitaxial growth into the holes. This approach has the advantage of using reasonably well understood materials technology to obtain the noncoplanar geometry as well as yielding an n^+-n contact which should substantially reduce the source resistance R_S. Disadvantages of this approach are that the drain and gate are still coplanar, good control over etching geometry must be achieved and maintained, and both insulating and moderately doped material must be grown in the presence of heavily doped n^+ GaAs. Nevertheless, the straightforwardness of this second approach is appealing in comparison to the alternate noncoplanar technology discussed earlier. Therefore, primary effort has been devoted to developing the technology to fabricate buried-insulating layer, noncoplanar FETs as will be discussed in the next section.

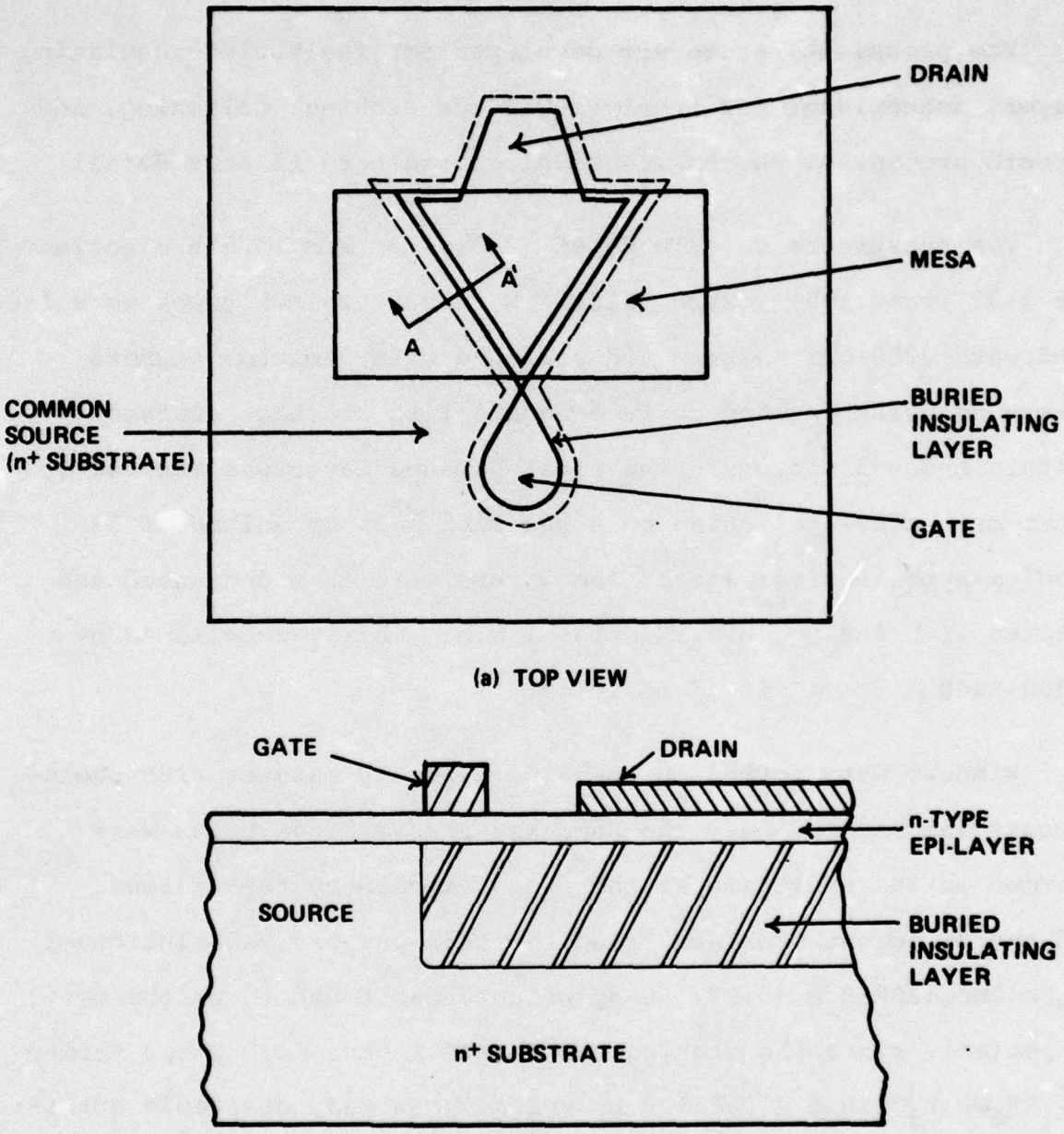


Fig. 2. Buried-insulating-layer noncoplanar FET.

3. MATERIAL AND DEVICE TECHNOLOGY DEVELOPED FOR BURIED-INSULATING-LAYER, NONCOPLANAR FET

The processing procedure developed for the buried-insulating-layer, noncoplanar FET involves various etching, polishing, and growth procedures which will be discussed here in some detail.

The substrates were Te doped (2-3 x $10^{18}/cm^3$) GaAs misoriented by 1-3° from (100) toward (110). Wafers 0.02-inch thick were lapped with 3200-grit slurry and polished with 3-micron diamond paste to bring the top surface parallel to the back surface within about 5 microns. The final damaged layer was removed by chem-mechanical polishing on a pad with 1:25 by volume of 5% sodium-hypochlorite:water. The wafers were then degreased and etched with 4 H_2SO_4:H_2O_2:H_2O for 1 min. This was followed by 4000-5000 Å thick SiO_2 deposition.

Windows were formed in the SiO_2 films by masking with photoresist and etching away the unmasked areas. Then holes were formed in the substrate at the areas exposed by the windows. Of the different etchants tried for this purpose, a solution of $K_3Fe(CN)_6$:KOH:H_2O (8:12:100 by weight) was found to be the best, especially since the etching was fairly isotropic. Holes formed by NH_4OH:H_2O_2:H_2O (20:7:500 by volume) has many desirable qualities, such as extremely smooth surfaces and sharp corners, but the etch rates for (111)A and B faces were quite different so that on one of the (110) cleavage faces the holes were dove-tailed.

The etching time was adjusted to give holes about 16 microns deep as shown in Fig. 3.

The holes were back-filled with oxygen-doped GaAs. In the presence of other impurities, probably Si or Zn, oxygen doping has been found to give high resistivity n-GaAs,[1] although the exact compensation mechanism is still unclear. The protective SiO_2 layer facilitated selective epitaxial deposition of GaAs in the holes.[2,3] The deposition process utilized a vapor phase reaction of Ga and GaAs with H_2 and $AsCl_3$ in an open flow system.[4,5] The different parameters affecting the growth of GaAs in this system have been analyzed elsewhere.[6] An excess amount of semi-insulating GaAs was deposited in the hole so that the top surface of the deposit was above the surface of the n^+ substrate, Fig. 4.

The wafers were then mounted on quartz plugs and the excess semi-insulating GaAs was repolished using 3-micron diamond paste. The polishing was stopped just when the diamond paste started removing the SiO_2 layer on the n^+ substrate. The SiO_2 layer was then stripped using dilute HF. The mechanical damage was removed by chem-mechanical polishing with dilute sodium-hypochlorite solution. Figure 5 shows such a repolished wafer etched with 10 H_2O:H_2O_2:HF to delineate the insulating regions.

Fig. 3. Etched hole, 16 microns deep on n^+-GaAs in (100) orientation. (Mag. 500x)

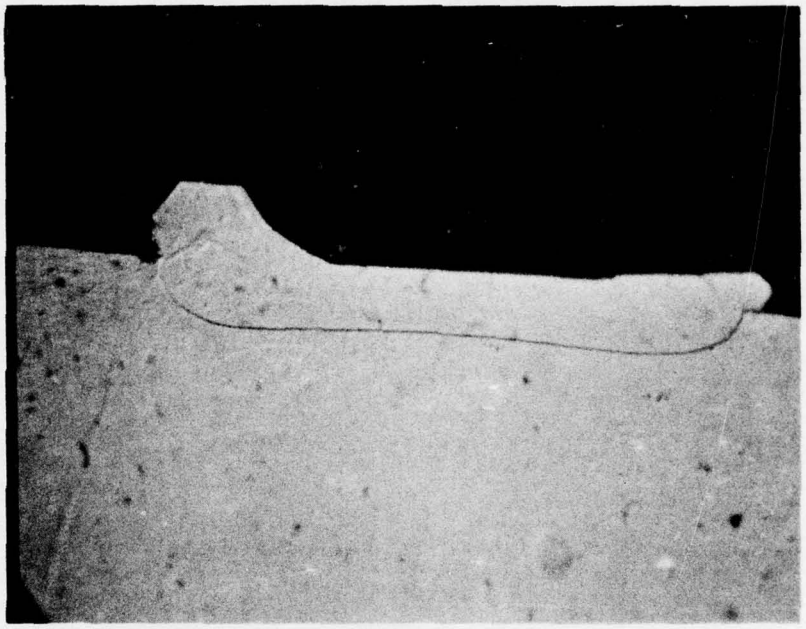


Fig. 4. Epitaxial n^- GaAs deposit in a hole etched in to an n^+ GaAs in (100) orientation. (Mag. 650x)

Fig. 5. Epitaxial n^- GaAs deposits in holes etched into an n^+ GaAs in (100) orientation, after the excess n^- deposits have been removed. The boundary has been revealed by a 10 H_2O: HF:H_2O_2 etch. (Mag. 80x)

After repolishing, the wafers were boiled in 5% KCN for 1 hr, rinsed in DI water and cleaned in isopropyl alcohol. Sub-micron thick n-type GaAs was deposited on these wafers in a vapor phase epitaxial reactor using $Ga/AsCl_3/H_2$ system. The Ga source contained Sn as the dopant. The use of such a system for uniform sub-micron epitaxial films has been demonstrated before.[7] The layers were typically about 0.3-micron thick doped to $10^{17}/cm^3$. A light 10 $H_2O:HF:H_2O_2$ etch prior to the deposition of this layer revealed the pattern even after the deposition of this layer (Fig. 6). This was necessary to aid alignment of the wafer during subsequent processing.

After active layer growth, processing to form FETs was begun. Mesas were etched across the insulating regions. Ohmic drain contacts were deposited and delineated by metal lifting techniques. The drain edge was aligned with the visible (by delineation) edge of the n^+ source beneath the active layer. The drain contacts were alloyed and drain current was measured. If required, the epitaxial layer was thinned slightly at this stage to provide the appropriate drain current. Schottky-barrier gate metallization was deposited and delineated by lifting. A gold contact overlay completed the device processing to produce a finished noncoplanar FET as shown in the photograph in Fig. 7.

Fig. 6. After the deposition of n-GaAs on the repolished wafer of Fig. 5. (Mag. 250x)

Fig. 7. Noncoplanar FET.

4. CHARACTERIZATION AND EVALUATION OF BURIED-INSULATING-LAYER, NONCOPLANAR FETs

A total of five wafers of buried-insulating-layer, noncoplanar FETs have been fabricated using the technology developed and described in the preceding section. The first wafer completed, NCT-1, exhibited devices with a field-effect transistor characteristic for the substrate biased positive and the drain electrode biased negative. This is, of course, the reverse bias polarity to that desired in order to operate with the substrate as common source. For a positive drain bias relative to the substrate, excessive drain current (breakdown) was obtained for drain bias in the range of 2-3 V as shown in Fig. 8. Since drain breakdown occurred below the saturation point, these devices did not perform well as microwave amplifiers. This same type of behavior has been observed on all noncoplanar FETs made with the oxygen-doped buried-insulating-layer technology.

The salient features of transistors assembled from wafer NCT-1 are typified by the data shown in Table I.

With the exception of unit 6, these devices were mounted in a 4-terminal package in order to operate with the drain grounded and the source (substrate) biased positively and acting as drain. This package has large parasitic capacitances and is no longer used for our other transistors. Since unit 6 could not be biased in saturation, the amplifier data are probably not indicative of the performance capability of these devices.

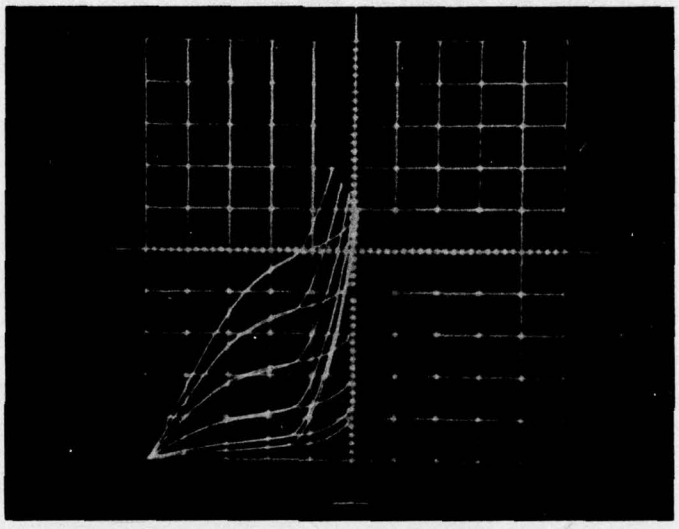


Fig. 8. Drain I-V characteristic of wafer NCT1-11 showing drain breakdown. Horizontal: 0.5 V/div; vertical: 10 mA/div; gate voltage steps 1 V.

TABLE I: NCT-1 Characteristics

(a) Curve Trace

Unit	I_{dss} (mA)	V_{dss} (V)	g_m (mmho)
1	50	2	13
2	58	2	15
6*	60	1.4	15 (@ V_{ds} = +2 V)
7	56	2	14
8	54	1.8	15
9	66	1.7	15
10	60	1.5	15

* bonded in forward direction (drain bias positive)

(b) Amplifier test @ 7 GHz

Unit	Gain (dB)
1	4.8
2	5.0
6	1.5
7	4.0
8	4.7
9	3.2
10	5.2

The second noncoplanar wafer was processed in two sections, NCT-2 and NCT-3. The first section, NCT-2, was well aligned as displayed in the photograph in Fig. 7. However, the epitaxial layer was too thick and no useful devices were obtained. The second section, NCT-3, was thinned prior to processing but required further thinning, and only a few devices were obtained.

Transistor NCT 3-1 was measured for source resistance, R_S, which was about 2.5 ohms. Microwave network analysis on NCT 3-1 yielded a transconductance g_m = 1.7 mmho and an output conductance g_{ds} = 1.6 mmho at 2 GHz. The input capacitance was about 0.57 pF. Calculated f_{max} was about 2 GHz and no attempt was made to test this device in an amplifier.

Wafer NCT-4 produced visually good transistors with I_{dss} of about 50-70 mA. However, the gate characteristic was soft and leaky, breaking down at about 4 V. The drain current could only be modulated by about 4 mA with a maximum gate bias of -4 V. This problem is believed to be caused by difficulties of growth of the active layer over the insulating region and associated interface problems.

Wafer NCT-5 was also fabricated using oxygen doping to obtain semi-insulating material for the buried-insulating-layer. After alloying of the drain contact, the current was about 140 mA so the wafer was lightly etched in 10 methanol:$2H_3PO_4$:$1H_2O_2$ which reduced the current to the range of 80-120 mA. After gate formation, however, the measured saturation current I_{dss} was in the range of 2-10 mA. This large decrease of current occurring at the gate deposition stage is not ordinarily observed. One possible explanation is that the higher current measured before gate deposition was carried in a thin heavily-doped layer near the insulating layer interface and that the slight amount of thinning

that occurs normally during gate fabrication due to cleaning, sputter etching, etc. thus greatly reduced the current. In spite of the reduced saturation, wafer NCT-5 exhibited drain breakdown voltage in the range of 3 to 6 V for positive drain bias as shown in Fig. 9. Several transistors were assembled from this wafer and tested with the results as shown in Table II. Curve trace characteristics of transistors from NCT-5 are shown in Figs. 9 and 10.

The calculated f_{max} from the measured admittance data was 7 GHz for unit 1 and 8 GHz for unit 3. The poor performance of transistors from NCT-5 can be attributed to low transconductance, high input capacitance, and high output conductance. In fact, input conductance (ReY_{11}) and the imaginary part of Y_{21}

TABLE II: NCT-5 Characteristics

1. Curve trace, R_s, and C_{gs} (1 MHz).

Unit	I_{dss}(mA)	V_{dss}(V)	g_m(mmho)	V_p(V)	R_s(Ω)	C_{gs}(pF)
1	9.6	1.6	4.4	4*	40.	0.39
2	2.4	1.2	1.5	2*	58.	0.40
3	4.8	1.4	4.0	3*	4.8	0.66
5	10.0	1.6	3.0	3*	16.	0.42

* Does not pinch off completely.

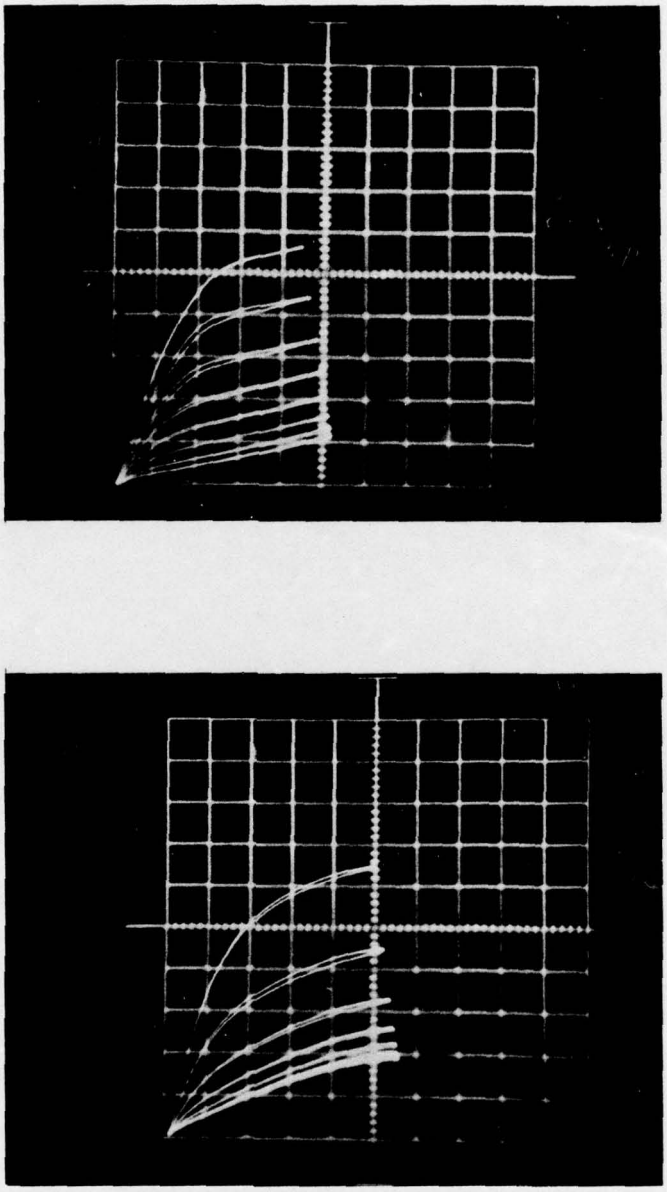


Fig. 9. Drain I-V characteristics from wafer NCT-5 units 1 and 3. Horizontal: 1 V/div, vertical: 2 mA/div (upper) and 1 mA/div (lower). Gate voltage steps 0.5 V.

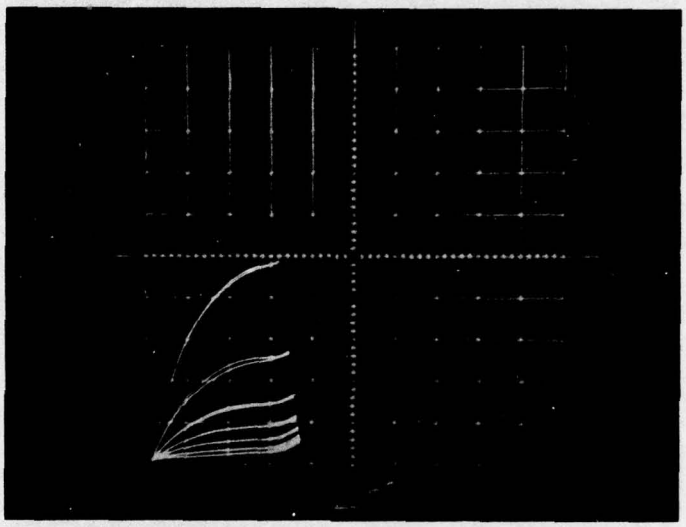


Fig. 10. Drain I-V characteristic of wafer NCT5-2. Horizontal 1 V/div, vertical 0.5 mA/div, gate voltage steps 0.5 V.

TABLE II (Contd.)

2. Microwave Network Analyzer (admittance in mmho).

	Im $Y_{11} \approx \omega C_{in}$		Re $Y_{21} \approx g_m$		Re $Y_{22} \approx g_{ds}$	
f(GHz)	1	3	1	3	1	3
2	5.2	6.0	4.5	5.9	0.65	0.52
3	6.7	8.2	4.4	5.6	0.81	0.70
4	9.3	11.5	4.4	5.6	0.99	0.89
5	12.2	15.3	4.9	6.4	1.69	1.69
6	14.0	18.0	4.9	6.3	2.05	2.16
7	18.1	23.2	5.1	6.4	2.67	3.29
8	21.8	28.3	6.4	8.1	4.27	5.10
9	25.6	32.9	6.4	7.8	7.67	9.81
10	28.7	37.0	7.6	8.7	15.22	22.14

3. Amplifier data:

	1	3
G(dB) at 4 GHz	3.	5.

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are also significantly higher for these transistors compared to equivalent-width coplanar GaAs transistors. These differences can all be traced to the properties of the buried-insulating-layer. In particular, the apparent increase of g_{ds} with frequency is not observed in devices fabricated on Cr-doped semi-insulating GaAs substrates and is indicative of shunting the output with a high capacitance RC-series branch.

The parasitic capacitance of the gate bonding pad over the buried insulating layer was calculated to be about 0.04 to 0.06 pF for a 10-micron deep insulating region. However, measurement of input capacitance for transistors from NCT-1, 3, and 5 indicates a range from 0.4 to 0.6 pF. The gate capacitance over the active layer is about 0.2 pF for n-layer doping of 1×10^{17} cm^{-3}. Therefore, the excess capacitance ranges between 0.2 and 0.4 pF or a factor of 3 to 10 higher than estimated. Three effects may be contributing to the increase of parasitic capacitance as follows:

(1) uneven polishing of the wafer surface after buried insulating layer growth;

(2) excessive vapor etching prior to active layer growth;

(3) out-diffusion of donor impurities from the n^+ substrate into the buried insulating layer during active layer growth.

The most straightforward solution to the excessive parasitic capacitance is to use deeper insulating regions under the gate and drain-bonding pads, minimize the bonding-pad size through improved wire-bonding techniques, and minimize high-temperature processing during active layer growth.

Drain breakdown also has been a major problem for the non-coplanar FETs fabricated to date. This problem reflects on the breakdown characteristics of the oxygen-doped semi-insulating layer. Breakdown in semi-insulating GaAs has been studied by

Haisty et al.[8] Undoped semi-insulating GaAs was shown to break down at the trap-filled-limit (TFL) as predicted by Lampert.[9] Only Cr-doped semi-insulating GaAs was shown to exhibit high breakdown under conditions of electron injection. More recently, the compensation mechanism of semi-insulating GaAs has been studied by Eisen et al.[10] Their conclusion is that both Cr and O doping are required to produce semi-insulating GaAs for which the Fermi level remains pinned at mid gap under injection of either holes or electrons. These studies appear to be relevant to the present work. The circumstances of drain breakdown under positive bias are quite analogous to the TFL breakdown observed in undoped semi-insulating GaAs.[8] The n^+ substrate would be injecting electrons into the oxygen-doped material under this bias condition. Under negative drain bias, the active layer would be attempting to inject electrons into the insulating material but the effect would be weaker due to lighter doping of the active layer compared to the substrate. Therefore, the TFL breakdown for negative drain bias would be substantially higher than for positive drain bias as observed. Since oxygen is a deep donor in GaAs[11] and since it must be weakly ionized (there are very few free electrons in the insulating layer), there are few electron traps (ionized oxygen donors) available in the insulating region. Therefore, the TFL is reached for a small electron injection under appropriate bias conditions and the device breaks down. The solution, of course, is to dope the insulating layer

with Cr to provide a deep acceptor to trap the injected electrons or alternately to dope with O plus a shallow acceptor at sufficient density to raise the TFL voltage. It is interesting that oxygen doping will produce insulating GaAs which is not, however, very useful for FET fabrication due to low breakdown voltage.

The other major problem observed in fabrication of buried-insulating-layer, noncoplanar FETs appeared to be associated with the interface properties between the insulating region and the active epitaxial layer (NCT-4). Various interface problems are notorious in the growth of FET material, even onto Cr-doped GaAs substrates. However, growth of uniformly doped active layers with high quality (abrupt) interfaces with the insulating regions in the noncoplanar geometry presents unique problems due to the presence of adjacent heavily n^+-doped substrate material. The magnitude of this problem is not apparent since only one of our 5 wafers exhibited a serious modulation problem. Various modifications of VPE growth procedures or the possibility of LPE growth of the final layer offer alternative approaches to minimizing the autodoping from the n^+ material and obtaining high quality interfaces.

5. CONCLUSIONS

The main conclusion to be reached from the work described in this report is that buried-insulator, noncoplanar FETs can be fabricated that will operation as amplifiers at microwave frequencies of 7 GHz or higher. Evaluation of the buried-insulating layer transistors fabricated has uncovered several problems which may be summarized as follows:

(a) low voltage drain breakdown for positive drain bias;

(b) excess parasitic capacitance and conductance on input and output of the transistor;

(c) nonzero pinch-off currents;

(d) nonmodulatable drain current (NCT-4 only).

The problem areas listed above can all be related to either the insulating (or noninsulating) properties of the O_2-doped layers or to the interfacial properties with the active layer. Specifically, problems (a) and (b) above could very likely be eliminated through use of Cr doping for the buried-insulating layer. Problems (c) and (d) are frequently observed on coplanar FETs fabricated on Cr-doped wafers and are, in any instance, not as severe in regard to degradation of transistor performance as the first two problems. Therefore, it is believed that high quality noncoplanar FETs can be made with the present buried-insulating layer process with the substitution of Cr doping for O_2 doping of the insulating regions and possibly some adjustment of the epitaxial process for the active layer to obtain satisfactory interface properties.

6. SUGGESTIONS FOR FUTURE WORK

The primary suggestion for future work is to improve the properties of the insulating material through the use of Cr doping. This would permit fabrication of single-element noncoplanar FETs with performance equivalent to or better than state-of-the-art coplanar low-noise FETs.

The work should, of course, be extended to the fabrication of parallel multi-element array power FETs. In this context, it appears that rectilinear geometrical pattern layout is preferential from the standpoint that crystallographic control of etching and regrowth properties should be obtainable in the ⟨100⟩ surface.[12] To this end, noncoplanar power FET masks have been designed and procured which use a parallel geometry for drain and gate fingers. This mask set was also designed with the capability of fabricating coplanar power FETs in mind so that ready comparison of characteristics and performance is possible.

Finally, the fully noncoplanar technology based on differential etching is still attractive for many reasons as described earlier. It was not found possible with the limited effort available on this program to pursue vigorously two alternate technologies simultaneously. The buried-insulating layer noncoplanar technology is presently better understood and closer to fruition than the alternate approach. However, the advantages of the fully noncoplanar dielectrically supported technology should also be explored.

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